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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/608,159	06/30/2000	Jeffrey R. Wilcox	42390.P8701	1109

7590 07/16/2004

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EXAMINER	
CAO, CHUN	

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 07/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/608,159	WILCOX ET AL.	
	Examiner	Art Unit	
	Chun Cao	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,12-15,22 and 23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,12-15,22 and 23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-4, 12-15, 22 and 23 are remained and presented for examination in this application.

2. The text of those applicable section of Title 35, U.S. Code not included in this action can be found in the prior Office Action.

Continued Examination Under 37 CFR 1.114

3. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 4/29/04 has been entered.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 2 and 4 are rejected under 35 U.S.C. 102(b) as being anticipated by Pathikonda et al. (Pathikonda). US patent no. 5,802,132.

As per claim 1, Pathikonda discloses that an integrated circuit comprises at least three cooperating frequency domains having variable operating frequencies [fig. 6B; col. 8, lines 39-54], wherein the at least three domains each operate at different frequencies

[fig. 6A; col. 8, lines 13-30]; cross-over logic to allow integral fractional ration frequency domain cross-over between more than one pair of frequency domains [col. 13, lines 27-32].

As per claim 2, inherently, Pathikonda discloses that cross-logic is capable of providing at least sixteen different cross-over ratios [col. 2, lines 32-40; col. 4, lines 40-49].

As per claim 4, Pathikonda inherently discloses a mask generator circuit to compute and generate masking signals for said cross-over logic on the fly using selectable cross-over ratios [col. 4, lines 40-65].

6. Claims 3, 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pathikonda et al. (Pathikonda). US patent no. 5,802,132 in view of Swoboda et al. (Swoboda), US Patent no. 5,329,471.

Swoboda is a prior art reference cited in prior office action.

As per claim 3, Pathikonda discloses of relations of number of frequencies [col. 4, lines 40-49]. Pathikonda does not explicitly disclose that at least three cooperating frequency domains comprise a processor domain and memory domain and a bus interface domain. However, Swoboda discloses at least three cooperating frequency domains comprise: a processor domain operable at a relatively large number of different frequencies; a memory control domain; a memory interface domain operable at a first relatively small number of frequencies; a bus interface domain operable at a second relatively small number of frequencies [fig. 52, col. 13, lines 42-65].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Pathikonda and Swoboda because they both disclose an integrated circuit having plurality of frequency domains and Swoboda discloses the limitations above would provide more functionality of Pathikonda's system by allowing to implement multiple flexible clock domain interface.

As to claims 12 and 13 are written in means plus function format and contain the same limitation as claims 1 and 3-4 in combination or respectively, therefore the same rejections applied.

7. Claims 14-15 and 22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pathikonda et al. (Pathikonda). US patent no. 5,802,132 in view of Fernando (Fernando), US Patent no. 5,471,587.

Fernando is a prior art reference cited in prior office action.

As per claim 22, Pathikonda discloses that an integrated circuit comprising: a first portion operable at a first plurality of frequencies said first portion to operate in a first frequency domain; a second portion operable at a second plurality of frequencies that are different to said first portion said second portion to operable in a second frequency domain; cross-over logic between said first portion and said second portion; a third portion operable at a third plurality of frequencies, said third portion to operate in a third frequency domain, wherein the first, second and third portions each operate at different frequencies [figs. 6A, 6B; col. 8, lines 13-54; col. 13, lines 27-32].

Fernando discloses that an integrated circuit having cross-over logic [6,8, fig. 1] to allow integral fractional ration frequency domain cross-over between more than one

pair of frequency domains [col. 1, 52-55; col. 3, lines 9-32]; and the cross-over logic comprising: a plurality of latches arranged as a FIFO array; a plurality of status bits comprise a plurality of free bits, a plurality of valid bits; a writer element to maintain a write pointer to said FIFO array in said first frequency domain; a reader element to maintain a read pointer to said FIFO array in said second frequency domain; domain crossing handshake circuitry to update said plurality of free bits and said plurality of valid bits [col. 5, lines 27-37; col. 6, line 28-col. 7, line 52; col. 10, lines 35-67].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Pathikonda and Fernando because they both disclose an integrated circuit having plurality of frequency domains and Fernando discloses the limitations above would improve the integrity of Pathikonda's system by allowing to implement detail limitations for the cross-over logic.

As the limitations set forth claim 23 is directed to implementations implementing the integrated circuit of claim 22. Fernando discloses a handshake circuitry [col. 6, lines 31-33]. As discussed above, Pathikonda and Fernando teach the integrated circuit of claim 22. It is for this reason, at the time of the invention, one of ordinary skill in the art would have readily recognized that Pathikonda and Fernando may obviously also teach the implementations of the integrated circuit of claim 22 as set forth in claim 23. Therefore, claim 23 is rejected under the same rationale with respect to claim 22.

As to claims 14-15 are written in means plus function format and contain the same limitations as claims 22 and 23 respectively, therefore the same rejections applied.

8. Applicant's arguments filed on 3/29/04, which have been considered but are moot in view of the new ground(s) of rejection.

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Nadeau-Dostie et al., US patent no. 6,115,827, discloses an integrated circuit comprises at least three clock domains each operates in different frequencies [col. 2, lines 16-18; col. 3, lines 57-64; col. 11, lines 17-18].

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun Cao at (703) 308-6106. The examiner can normally be reached on Monday-Friday from 7:30 am - 4:00 pm. If attempts to reach the examiner by phone are unsuccessful, the examiner's supervisor Thomas Lee can be reached at (703) 305-9717. The fax number for this Art Unit is following: Official (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 306-5631.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chun Cao

July 12, 2004